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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,080	08/28/2003	Hajime Kimura	12732-162001/ US6582	7214

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FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
NGUYEN, KIMNHUNG T	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,080	KIMURA ET AL.	
	Examiner	Art Unit	
	Kimnhung Nguyen	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/8/04, 2/5/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Application has been examined. The claims 1-15 are pending. The examination results are as following.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Dawson et al. (US 6,229,506).

Regarding claims 1 and 9, Dawson et al. discloses in figs. 2, 4 a current source circuit (230) comprising: plural transistors (250, 260, 270); means for switching series and parallel connections of the plural transistors 250, 260, 270); means for converting a first current (260) input through the plural transistors to voltage (see col. 3, lines 55-64); means for holding the converted voltage (C280); means for converting the held voltage to a second current (from TFT 270); and means for supplying the converted second current (TFT 270) to an object to be driven.

Regarding claim 2, Dawson et al. discloses in figs 2, 4, a current source circuit comprising: plural transistors (250, 260, 270); means for switching series and parallel connections of the plural transistors (25, 260, 270); means for converting a first current input

(260) through the plural transistors to voltage (see col. 3, lines 55-64); means for holding the converted voltage (C280); means for converting the held voltage to a second current (270); and means for supplying the converted second current to an object to be driven, wherein the plural transistor (25, 260, 270) are connected in series when current is supplied to the object to be driven, while the plural transistors are connected in parallel when the first current is converted to voltage.

Regarding claim 10, Dawson et al. discloses in fig. 2, a display device comprising a scanning line (210) a signal line (220) to which digital signals are input; a light emitting element (LED pixel) provided at the intersection position of the scanning line and the signal line, and current source circuit (230) for supplying current to the light emitting element, wherein the current source circuit has plurality transistors (250, 260, 270).

3. Claims 3, 5-6, 8 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Stewart et

al. (US 5,952,789).

Regarding claims 3 and 6, Stewart et al. discloses in fig. 5, a current source circuit comprising: a first transistor and a second transistor (T1, T2); a capacitor element (C1) connected to the gate electrodes (S1) of the first transistor (T1) and the second transistor (T2); a power source line (see switching power line) connected to one end of the capacitor element (C1); a current source line (fig. 5) connected to the other end of the capacitor element (C1); and means

for supplying electric charges held in the capacitor element (C1) as current to an object to be driven.

Regarding claims 5 and 8, Stewart et al. discloses the first and second transistors are an inherent of organic transistors (because they drive the circuit).

Regarding claim 11, Stewart et al. discloses in fig. 5, a method for driving a current source circuit having a first transistor (T1), a second transistor (T2), a capacitor element (C1, C2) connected to the gate electrodes of the first transistor and the second transistor and a current source line (fig. 5) and power source line (see switching power line) connected to the capacitor element (C1, C2), the method comprising the steps of: feeding current supplied from the power source line to the power source line through the first transistor and second transistor, which are connected in parallel; and feeding current from the power source line to an object to be driven through the first transistor and second transistor, which are connected in series.

Regarding claim 12, Stewart et al. discloses in fig. 5, a method for driving a current source circuit having a first transistor (T1), a second transistor (T2), a capacitor clement (C1, C2) connected to the gate electrodes of the first transistor and the second transistor and a current source line (fig. 5) and power source line (see switching power line) connected to the capacitor element, the method comprising the steps of: connecting the first transistor and second transistor in parallel when a setting operation is performed on the first transistor and second transistor; and connecting the first transistor and second transistor in series when current is supplied from the first transistor and second transistor to an object to be driven.

Regarding claims 13-14, Stewart et al. discloses in fig. 5, a method for driving a current source circuit having a first transistor, a second transistor, a capacitor element connected to the gate electrodes of the first transistor (T1) and the second transistor (T2) and a current source line and power source line connected to the capacitor element, the method comprising the steps of: feeding current to the capacitor element (C1, C2) and holding electric charges such that the capacitor element can feed a predetermined amount of voltage (see col.7, lines 34-51); supplying current based on the predetermined amount of voltage to the first transistor and second transistor, which are connected in parallel, such that the transistors can feed a predetermined amount of current; and supplying the predetermined amount of current to an object to be driven through the first transistor and second transistor, which are connected in series (fig. 5).

4. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Imamura (US 2003/0133243).

Regarding claim 15, Imamura discloses in figs. 9, 12, a method for driving a display device, the display device including: plural scanning lines (Yn); plural signal lines (Xm) to which digital signals are input; light emitting element (61) provided at the intersection positions of the scanning lines and the signal lines; and a current source circuit (64) for supplying current to the light emitting elements, the method comprising the steps of: dividing a unit frame period (figs. 4a-4b) corresponding to an synchronizing timing of video signals input to the signal line into m sub frame periods, SFI, SF2... and SFm (where m is a natural number of two or larger) and providing at least one of the m sub-frame periods SFI, SF2..., and SFm with an erasing time;

and performing a setting operation on the current source circuit in the erasing time (see second sub-frame, display-off codes and this period, the organic EL elements are prevented from emitting light, see[0074], [0086]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stewart et al. (US 5,952,789) in view of Yamagishi et al. (US 6,501,466 cited by Applicant).

Stewart et al. does not disclose the first, the second and the third transistors are P-channel. Yamagishi et al. discloses in fig. 1, a current source system having the first, the second and the third transistors are P-channel type (see col. 11, lines 19-29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the using of the first, the second and the third transistors are P-channel as taught by Yamagishi et al. into the system of Stewart et al. because this would be selectively injected into the channel in order to shift the threshold voltage toward the enhancement side, which also less expensive to fabricate (see col. 11, lines 23-27).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimnhung Nguyen whose telephone number is (571) 272-7698. The examiner can normally be reached on MON-FRI, FROM 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimnhung Nguyen
November 5, 2005

AMR A. AWAD
PRIMARY EXAMINER